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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,061	02/11/2004	Manish Sharma	200310026-1	2092
22879	7590	10/18/2005		
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400				
			EXAMINER SOFOCLEOUS, ALEXANDER	
			ART UNIT 2824	PAPER NUMBER

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

18

Office Action Summary	Application No. 10/776,061	Applicant(s) SHARMA, MANISH	
	Examiner Alexander Sofocleous	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>(1) 2/11/2004</u> | 6) <input checked="" type="checkbox"/> Other: <u>Search History</u> |

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 11, 2004, and the Information Disclosure Statement filed on February 11, 2004.
2. Claims 1-16 are pending in the case. Claims 1, 12, and 13 are independent claims.

Specification

3. The disclosure is objected to because of the following informalities: There are two spellings of "magnetization." On page 1, line 21 (paragraph 0003), the word is spelled "magnetisation." Several other locations support this spelling. On page 2, line 1 (paragraph 0004), the word is spelled "magnetization." Although 37 CFR 1.52 (b) (1) (ii) only requires the disclosure to be in English and does not specify that it must be American English, it is suggested that applicant choose one spelling for the word. Examiner suggests replacing all instances of the word "magnetisation" with the word "magnetization" in order to maintain consistency in the application.
4. On page 6, line 20-21, the specification indicates that the **data layer is 212** and the **reference layer is 208**. Examiner assumes that applicant intended for the **reference layer to be 212** and the **data layer to be 208**.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran U.S. Patent 6,865,105B1 in view of Ohmori U.S. Patent 6,920,065B2.

Regarding independent claim 1-3 and 12, Tran teaches a computer system comprising a central processing unit, a main board, and a thermally assisted memory connected to the mainboard (not shown in figures; see column 4, lines 42-46). The memory forms a cross-point array with a plurality of conductive rows (Fig. 2 [102,202]), a plurality of conductive columns (Fig. 2 [104, 206, 208]), and memory cells (Fig. 2 [100, 100', 210, 212, 214, 216]) at the cross-points (see column 6, lines 11-14). The memory cells have a reference layer (Fig. 1 [110]) that can be a soft reference layer (column 6, lines 43-44) and a data layer (Fig. 1 [106]). The data layer is switchable between two magnetic states. The reference layer, being a soft reference layer, is switchable between two magnetic states. The current needed to alter the magnetization state of the reference layer is small enough such that the same current will not alter the magnetization state of the data layer (column 6, lines 52-54); therefore, the coercivity of the reference layer is smaller than the coercivity of the data layer. The data layer in this instance has not been heated. During a write operation, the magnetic field applied to

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the memory cell is strong enough to overcome the coercivity of the cell when heated, yet, not strong enough to overcome the coercivity of the cell when unheated (column 8, lines 25-27). Therefore, the coercivity of the data layer is higher than the coercivity of the reference layer. The data layer is heated and its coercivity is still higher than the coercivity of the reference layer. The heating of the data layer reduces the coercivity of the data layer such that the coercivity of the heated data layer is lower than the coercivity of the reference layer. However, Tran is silent with respect to the heating element proximate to the data layer.

Ohmori shows that the data layer (Fig. 1 [13]) is heated by a resistance heater (Fig. 1[21]), or heating element, that is proximate to the data layer in order to reduce the coercive force of the data layer (column 18, lines 7-10). Resistance heater and heating element are synonymous in this context. Furthermore, it is evident with respect to the claim limitations discussed above that the data layer has a higher coercivity than the reference layer at an initial temperature. As the data layer is heated, the coercivity of the data layer decreases (column 18, lines 7-10) from the initial coercivity, which is still higher than the coercivity of the reference layer; and, eventually is heated to a temperature such that the coercivity of the data layer is lower than the coercivity of the reference layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori, with respect to adding a heating element proximate to the data layer of the memory device of Tran such that the data layer is heated by the heating element in order to reduce the coercive force of the data layer

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(Ohmori column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori and Tran are from the same field of endeavor such as being MRAM with memory cells that have a data layer, reference layer, and intermediate layer and also being classified under U.S. Cl. 365 (static memories).

As per **claim 13**, it encompasses the same scope of invention as to that of claim 1 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 4, Tran teaches all of the claim elements discussed above. Tran is silent with respect to the heating element being a heat-inducing layer.

Ohmori teaches all of the claim elements discussed above and additionally, teaches that the data layer (Fig. 1 [13]) is heated by a resistance heater (Fig. 1[21]), or heating element; i.e., the resistance heater is a layer that induces heat to the data layer. Therefore, the resistance heater is a heat-inducing layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori, with respect to adding a heating element, that is a heat-inducing layer, proximate to the data layer of the memory device of Tran such that the data layer is heated by the heating element in order to reduce the coercive force of the data layer (Ohmori column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori and Tran are from the same field of endeavor such as being MRAM with memory cells that have a

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data layer, reference layer, and intermediate layer and also being classified under U.S. Cl. 365 (static memories).

As per **claim 14**, it encompasses the same scope of invention as to that of claim 4 except it drafts in method format instead of apparatus format. The electric current is made flow through the first wiring 22 to heat the storage layer 13 by the resistance heater 21 (Ohmori column 10, lines 16-18). Or, in summary, the current is applied through the wires to the heater in order to generate heat. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 5, Tran teaches all of the claim elements discussed above. Tran is silent with respect to the heat-inducing layer being a resistive layer.

Ohmori teaches all of the claim elements discussed above and additionally teaches a resistance heater, that is already shown to be a heat-inducing layer, which is a resistance, or resistive, layer. Therefore, the heat-inducing layer is a resistive layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori, with respect to adding a heating element, that is a heat-inducing layer that is a resistive layer, proximate to the data layer of the memory device of Tran such that the data layer is heated by the heating element in order to reduce the coercive force of the data layer (Ohmori column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori and Tran are from the same field of endeavor such as being MRAM

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with memory cells that have a data layer, reference layer, and intermediate layer and also being classified under U.S. Cl. 365 (static memories).

As per **claim 15**, it encompasses the same scope of invention as to that of claim 5 except it drafts in method format instead of apparatus format. The electric current is made flow through the first wiring 22 to heat the storage layer 13 by the resistance heater 21 (Ohmori column 10, lines 16-18). Or, in summary, the current is applied through the wires to the heater in order to generate heat. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 11, Tran shows that prior art teaches that memory cells may be a tunneling magneto-resistive memory cell, or TMR (Tran column 1, lines 37-38).

5. Claims 1-5, and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner U.S. Patent Application No. 2005/0169034A1 in view of Ohmori U.S. Patent 6,920,065B2.

Regarding independent claim 1-3 and 12, Perner teaches a computer system with a main board, CPU and at least one memory store comprised of an embodiment of the memory device (not shown in figures; see paragraph 0064). Perner shows a cross-point array (Fig. 5 [302]) of resistive devices (Fig. 5 [500, 506, 508...520]) where the cross-point array comprises a plurality of word lines, or conductive columns, and a plurality of bit lines, or conductive rows (paragraph 0006). Perner also shows that the resistive devices are SVM cells that comprise at least one ferromagnetic data layer (Fig.

4 [402]), an intermediate layer (Fig. 4 [404]), and a ferromagnetic reference layer (Fig. 4 [406]). The data layer stores 1-bit of data as an alterable orientation of magnetism (paragraph 0038); i.e., the data layer is switchable between two states under the influence of magnetism. Perner shows the reference layer is a soft-reference layer and accommodates two states (Fig. 4 [M2 on block 400] and [M2 on block 400']). Furthermore, Perner shows that the reference layer has a lower coercivity than the data layer (paragraph 0039). However, Perner does not show a heating element proximate to the data layer that is used to heat the data layer so as to reduce the coercivity of the data layer.

Ohmori teaches that the data layer (Fig. 1 [13]) is heated by a resistance heater (Fig. 1[21]), or heating element, that is proximate to the data layer in order to reduce the coercive force of the data layer (column 18, lines 7-10). Resistance heater and heating element are synonymous in this context. Furthermore, it is evident with respect to the claim limitations discussed above that the data layer has a higher coercivity than the reference layer at an initial temperature. As the data layer is heated, the coercivity of the data layer decreases (column 18, lines 7-10) from the initial coercivity, which is still higher than the coercivity of the reference layer; and, eventually is heated to a temperature such that the coercivity of the data layer is lower than the coercivity of the reference layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori, with respect to adding a heating element proximate to the data layer of the memory device of Perner such that the data layer is

heated by the heating element in order to reduce the coercive force of the data layer (Ohmori column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori and Perner are from the same field of endeavor such as being MRAM with memory cells that have a data layer, reference layer, and intermediate layer and also being classified under U.S. Cl. 365 (static memories).

As per **claim 13**, it encompasses the same scope of invention as to that of claim 1 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 4, Perner teaches all of the claim elements discussed above. Perner is silent with respect to the heating element being a heat-inducing layer.

Ohmori teaches all of the claim elements discussed above and additionally, teaches that the data layer (Fig. 1 [13]) is heated by a resistance heater (Fig. 1[21]), or heating element; i.e., the resistance heater is a layer that induces heat to the data layer. Therefore, the resistance heater is a heat-inducing layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori, with respect to adding a heating element, that is a heat-inducing layer, proximate to the data layer of the memory device of Perner such that the data layer is heated by the heating element in order to reduce the coercive force of the data layer (Ohmori column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori and Perner are

from the same field of endeavor such as being MRAM with memory cells that have a data layer, reference layer, and intermediate layer and also being classified under U.S. Cl. 365 (static memories).

As per **claim 14**, it encompasses the same scope of invention as to that of claim 4 except it drafts in method format instead of apparatus format. The electric current is made flow through the first wiring 22 to heat the storage layer 13 by the resistance heater 21 (Ohmori column 10, lines 16-18). Or, in summary, the current is applied through the wires to the heater in order to generate heat. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 5, Perner teaches all of the claim elements discussed above. Perner is silent with respect to the heat-inducing layer being a resistive layer.

Ohmori teaches all of the claim elements discussed above and additionally teaches a resistance heater, that is already shown to be a heat-inducing layer, which is a resistance, or resistive, layer. Therefore, the heat-inducing layer is a resistive layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori, with respect to adding a heating element, that is a heat-inducing layer that is a resistive layer, proximate to the data layer of the memory device of Perner such that the data layer is heated by the heating element in order to reduce the coercive force of the data layer (Ohmori column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori and Perner are from the same field of endeavor such as being MRAM

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with memory cells that have a data layer, reference layer, and intermediate layer and also being classified under U.S. Cl. 365 (static memories).

As per **claim 15**, it encompasses the same scope of invention as to that of claim 5 except it drafts in method format instead of apparatus format. The electric current is made flow through the first wiring 22 to heat the storage layer 13 by the resistance heater 21 (column 10, lines 16-18). Or, in summary, the current is applied through the wires to the heater in order to generate heat. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 11, Perner shows that prior art teaches that memory cells may be a tunneling magneto-resistive memory cell, or TMR (paragraph 0004).

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. **Claims 1-16 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of copending Sharma U.S. Patent Application No. 2005/0173771A1 in view of Ohmori U.S. Patent No, 6,920,065B2.** Although the conflicting claims are not identical, they are similar except that Sharma '828A1 is drawn to heating the data layer while Sharma '771A1 is drawn to heating the reference layer. Ohmori '065B2 shows that the data layer (Ohmori '065B2 Fig. 1 [13]) is heated by a heating element (Ohmori '065B2 Fig. 1[21]) that is proximate to the data layer.

This is a provisional obviousness-type double patenting rejection.

Regarding independent claim 1, Sharma '771A1's claim 1 shows an MRAM device comprising: a plurality of magnetic memory cells; a plurality of word and bit lines connecting columns and rows of the memory cells, each memory cell having a magnetic reference layer and a magnetic data layer, each magnetic reference layer and each magnetic data layer having a magnetization being switchable between two states under the influence of a magnetic field; and a plurality of heating elements each proximate to a respective reference layer, each heating element in use providing for localized heating of the respective reference layer so as to facilitate switching of the reference layer. Sharma '771A1's claim 2 shows that, at a first temperature, the reference layer is of a lower coercivity than the data layer. However, Sharma '771A1 is drawn to heating the reference layer instead of heating the data layer. Ohmori '065B2 shows that the data layer (Ohmori '065B2 Fig. 1 [13]) is heated by a heating element (Ohmori '065B2 Fig. 1[21]) that is proximate to the data layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori '065B2, with respect to adding a heating element proximate to the data layer of the memory device, as opposed to adding a heating element proximate to the reference layer, in a way similar to Sharma '771A1 such that the data layer is heated by the heating element in order to reduce the coercive force of the data layer (Ohmori '065B2 column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori '065B2 and Sharma '771A1 are from the same field of endeavor such as being MRAM with memory cells that have a data layer, reference layer, and intermediate layer, involving heating a layer of the memory cell, and also being classified under U.S. Cl. 365 (static memories).

Regarding dependent claim 2, it is evident with respect to the claim limitations discussed above that the data layer has a higher coercivity than the reference layer at an initial temperature. As the data layer is heated, the coercivity of the data layer decreases (Ohmori '065B2 column 18, lines 7-10) from the initial coercivity, which is still higher than the coercivity of the reference layer.

Regarding dependent claim 3, it is evident with respect to the claim limitations discussed above that heating the data layer, in order to lower the coercivity of the data layer (Ohmori '065B2 column 18, lines 7-10), eventually results in the coercivity of the data layer decreasing lower than that of the reference layer.

Regarding dependent claims 4-8, Sharma '771A1's claims 3-5 and 7-8 further recite additional limitations that are the same as those in present claims 4-8.

Regarding dependent claims 9-10, Sharma '771A1's claims 6 and 9 further recite additional limitations that are the same as those in present claims 9-10.

Regarding dependent claim 11, Sharma '771A1's claim 10 further recite additional limitations that are the same as those in present claim 11.

Regarding independent claims 12, Sharma '771A1's claim 11 combined with Sharma '771A1's claim 2 further recites additional limitations that are the same as those in present claim 12. However, Sharma '771A1 is drawn to heating the reference layer instead of heating the data layer. Ohmori '065B2 shows that the data layer (Ohmori '065B2 Fig. 1 [13]) is heated by a heating element (Ohmori '065B2 Fig. 1[21]) that is proximate to the data layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori '065B2, with respect to adding a heating element proximate to the data layer of the memory device, as opposed to adding a heating element proximate to the reference layer, in a way similar to Sharma '771A1 such that the data layer is heated by the heating element in order to reduce the coercive force of the data layer (Ohmori '065B2 column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori '065B2 and Sharma '771A1 are from the same field of endeavor such as being MRAM with memory cells that have a data layer, reference layer, and intermediate layer, involving heating a layer of the memory cell, and also being classified under U.S. Cl. 365 (static memories).

Regarding claims 13-16, Sharma '771A1's 12-15 further recite additional limitations that are the same as those in present claims 13-16, except for the data layer being heated. Ohmori '065B2 shows that the data layer (Ohmori '065B2 Fig. 1 [13]) is heated by a heating element (Ohmori '065B2 Fig. 1[21]) that is proximate to the data layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ohmori '065B2, with respect to adding a heating element proximate to the data layer of the memory device, as opposed to adding a heating element proximate to the reference layer, in a way similar to Sharma '771A1 such that the data layer is heated by the heating element in order to reduce the coercive force of the data layer (Ohmori '065B2 column 18, lines 7-10). Further motivation to perform the above stated modification are evidenced by the fact that both Ohmori '065B2 and Sharma '771A1 are from the same field of endeavor such as being MRAM with memory cells that have a data layer, reference layer, and intermediate layer, involving heating a layer of the memory cell, and also being classified under U.S. Cl. 365 (static memories).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Smith et al. U.S. Patent Application 2005/0052902A1, Sharma et al. U.S. Patent Application No. 2003/0202375A1, Tran et al. U.S. Patent Application No. 2003/0058684A1, Tran et al. U.S. Patent 6,504,221B1, and Tran U.S. Patent Application No. 2005/0063223A1.

Smith et al. '902A1 shows a MRAM in which the memory cells have a fixed (reference) layer and a non-fixed (data) layer. During write operations, a bias voltage is applied across a set of conductors to produce a current through a dielectric layer that will result in the reference layer, or data layer, to increase in temperature due to Joule heating. The reference layer and data layer positioning are not predetermined in this application (see paragraph 0021). However, this application does not include a separate heating element to heat such layers.

Sharma et al. '375A1 shows a MRAM in which the memory cells have a reference layer, a sense layer (data layer), and insulating tunnel barrier (intermediate layer). The memory cells can be TMR (tunneling magneto-resistive) or SDT (spin dependent tunneling junction). The reference layer can be made using a soft magnetic layer. The tunneling barrier is typically made of alumina or silicon dioxide. This application does not mention heating the data layer.

Tran et al. '684A1 shows a MRAM in which the memory cells have a reference layer, and a data layer. The reference layer can have magnetization oriented in either of two directions. The data layer can have magnetization oriented in either of two

directions. The coercivity of the data layer is greater than the coercivity of the reference layer. This application does not mention heating the data layer.

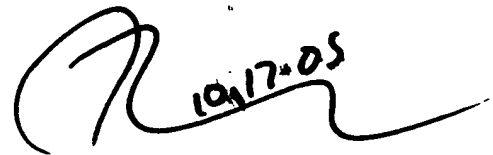
Tran et al. '221B1 shows a MRAM in which the memory cells have a reference layer, and a data layer. The memory cells can be TMR (tunneling magneto-resistive) or SDT (spin dependent tunneling junction). The reference layer can be made using a soft magnetic layer and that the coercivity of the reference layer is lower than the coercivity of the data layer. This patent does not mention heating the data layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS



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